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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,797	12/29/2005	Susumu Kasukabe	500.45763X00	8707

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EXAMINER	
ISLA RODAS, RICHARD	
ART UNIT	**PAPER NUMBER**
2829	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/562,797	KASUKABE ET AL.	
	Examiner	Art Unit	
	Richard Isla-Rodas	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18,19 and 21-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18,19,21-25,27 and 28* is/are rejected.

7)☒ Claim(s) *26 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 24 and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Dasse #5,399,505 (Dasse hereinafter) in view of the US Patent to Liu et al. #5,847,571 (Liu hereinafter).

In terms of claims 24 and 27, Dasse teaches in Figure 7, a method including the steps of building a circuit in a wafer and forming a plurality of semiconductor elements (steps 132+133), performing electrical testing on the semiconductor devices (137) and dicing and separating the wafer into the semiconductor elements (see step 162 in Figure 8).

Dasse et al. substantially teaches the method steps except for the preferred structure with which to perform the step of testing. That is, Dasse teaches the method as claimed except for using a probe card including contact terminals formed within a first area surrounded by a first metal film of a probe sheet, wherein the electrical characteristics of each of the semiconductor elements are tested by pushing the first area surrounded by the first metal film while fixing a second metal film formed so as to surround the first metal film of the probe sheet thereby to make the plurality of the contact terminals contact with the electrodes of the semiconductor element.

Liu teaches a method of testing semiconductors elements by contacting electrodes of a semiconductor device (such as the electrode 8 in figure 1d) using contact terminals (such as elements 44 in Figure 5) of a probe card (Figure 2 shows a view of the membrane probe card shown in for example, Figures 1a, 1b and 1c) having a probe sheet (element 10 in Figure 5), wherein the contact terminals are formed within a first area surrounded by a first film (element 32 in figure 2), and wherein the semiconductors are tested by pushing the first area (by using for example, element 25 in Figure 1d) while fixing a second film (element 64 in Figure 3) in place. It would have been obvious to one of ordinary skill in the art at the time the invention was made, to choose the readily available interface probe card disclosed by Liu, to perform the method steps (testing) in the method taught by Dasse, in order to prevent damaging the electrodes in the semiconductor during testing since the probe sheet is resilient and flexible and avoids the application of excessive pressure on the electrodes.

Also, Liu substantially teaches the method steps except for the preferred material with which to manufacture the first and second films. That is, Dasse teaches the method as claimed except for using metal for parts 58 and 64. However, since both metal film in the present application and the PCB films used in Liu's device serve the same purpose (supporting for the contacting elements), it would have been obvious to use a the preferred material (metal) over the material used by Liu (most probably silicon) in the basis of its suitability, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshi, 125 USPQ 416. That

is, one of ordinary skill in the art would have recognized that silicon structures may be replaced by metal structures and vice versa, as both materials offer the same capability of support.

As to claim 21, Liu teaches a pushing mechanism (22) that applies pressure to an area formed with the first metal film (32) and an area formed with the plurality of contact terminals of the probe sheet (10) as explained in lines 5-9 of column 4. The electrical characteristics of each semiconductor element are tested by pushing the probe sheet (using pressure means 22) and allowing the probes (44 in shown in figure 5) to contact the electrodes (elements 8, shown in for example, Figure1d).

3. Claims 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Dasse in view of Liu and further in view of Liu et al. #5,177,439 (Liu #439 hereinafter).

As to claims 18 and 22, Dasse in view of Liu substantially shows all of the claimed method steps except for the use of contact terminals that are pyramidal in shape. The use of pyramidal contact terminals is however, well known in the art, as exemplified by Liu #439. In figure 4, Liu #439, shows a probe card (8) including contacts (15) in the shape of pyramids. It would have been obvious to one of the ordinary skill in the art, at the time of the invention, to use the teachings of pyramidal contacts as disclosed by Liu #439 to design the probes in the device disclosed by Liu as pyramids in order to penetrate any superficial oxide present on the electrode pads or bumps of the semiconductor device to be tested, as suggested in lines 50-54 of column

4. Claims 19 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Dasse in view of Liu and further in view of Maddix et al. #6,232,143 (Maddix hereinafter).

In terms of claims 19 and 23, Dasse in view of Liu teaches all of the claimed elements as discussed above except for the step of forming the contact terminals using as a mold member, the holes formed by anisotropic etching of a crystalline board. Instead, Liu teaches that the probes may be formed by anisotropic wet etching. However, step of making probe tips by using molds is well known in the art. For example, Maddix teaches in lines 4-7 of the abstract, a method of molding probe points on molds constructed by etching pits onto silicon wafers. As described in Claim 6 of Maddox's patent (lines 19-21 in column 10), said silicon wafer may be a monocrystalline silicon (also see lines 65-67 in column 1 and 1-2 in column 2). It would have been obvious to one of the ordinary skill in the art, at the time of the invention, to use the teaching of probe tip manufacture by way of etching molds on crystalline bards as disclosed by Maddix, to manufacture the probes through said process in the device disclosed by Liu in order to improve the range of sizes the probe assembly is capable of contacting, since molding as taught by Maddix, yields a fine probe point which in turn is capable of contacting smaller devices as suggested in lines 61-65 of column 2.

5. Claims 25 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Dasse in view of Liu and further in view of DiStefano. #6,426,638 (DiStefano hereinafter).

In terms of claims 25 and 28, Dasse in view of Liu substantially teaches all of the claimed elements as discussed above except for constructing some elements (namely the first metal film) with a linear expansion coefficient that is substantially the same as the wafer under test. However, manufacturing parts of a tester, and specifically probe card pieces to follow a coefficient of expansion that is similar to that of the wafer tested, is well known in the art. For example DiStefano teaches in figure 4A, a probe system in which support member 61 and 62 are constructed of coefficient of expansion that are similar to that of the wafer being tested (see lines 18-19 in column 3). It would have been obvious to one of the ordinary skill in the art at the time the invention was made, to use the teachings of manufacturing most parts of a testing system to follow the same coefficient of expansion as the device under test as disclosed by DiStefano, to manufacture the metal film in Liu's device with a coefficient of expansion similar to that of the wafer being contacted, in order to account for expansions due to heating produced during the testing process which could potentially misalign the probes with respect to the electrodes in the wafer of Liu's device.

Allowable Subject Matter

6. Claims 26 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In terms of claims 26, the prior art of record does not teach alone or in combination a method of producing a semiconductor device including the step of

contacting a plurality of contact terminals formed within a first area surrounded a first metal film, wherein the first metal film has a linear expansion coefficient substantially the same as a linear expansion coefficient of the wafer and is formed by 42 alloy or invar, in combination with all other elements in claim 26.

In terms of claims 26, the prior art of record does not teach alone or in combination a method of producing a semiconductor device including the step of contacting a plurality of contact terminals formed within a first area surrounded a first metal film, wherein the first metal film has a linear expansion coefficient substantially the same as a linear expansion coefficient of the wafer and is formed by 42 alloy or invar, in combination with all other elements in claim 26.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Document Number Number-Kind Code e.g. 0500004 A1	Date MM-YYYY	Name	Classification
6,379,982	04-2002	Ahn et al.	438/14
5,621,333	04-1997	Long et al.	324/762
5,973,504	10-1999	Chong, Fu Chiung	324/754

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Isla-Rodas whose telephone number is (571) 272-5056. The examiner can normally be reached on Monday through Friday 8 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Richard Isla-Rodas
December 5, 2007

HA TRAN NGUYEN
SUPERVISORY PATENT EXAMINER